

CS 315-02 Digital Logic Components

Lab 08 Testing

gates $\neg$ $\wedge$ $\vee$ $\rightarrow$ $\leftrightarrow$

wires, inputs, outputs, splitter/merger

combinational logic

1) Outputs depend only on the inputs

2) A circuit without cycles
a DAG $\rightarrow$ Directed Acyclic Graph

sum-of-products

boolean algebra equation $\rightarrow$ circuit

adder - ripple-carry adder

circuit as components

project 05 $\rightarrow$ static analyzer

Comparator

is $a == b$?

$$eq = (\bar{a} \cdot \bar{b}) + (a \cdot b)$$

	a	b	eq
✓	0	0	1
	0	1	0
	1	0	0
✓	1	1	1

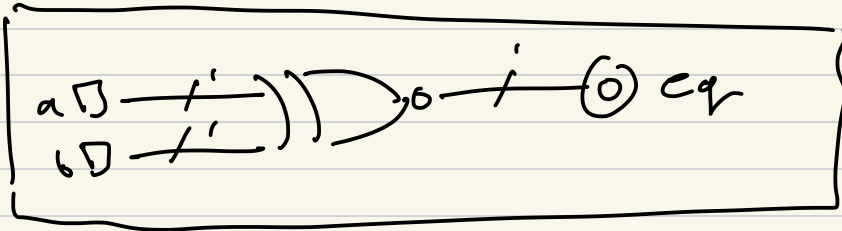
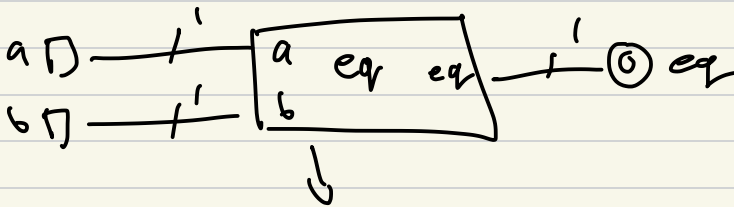
XOR

0
1
1
0

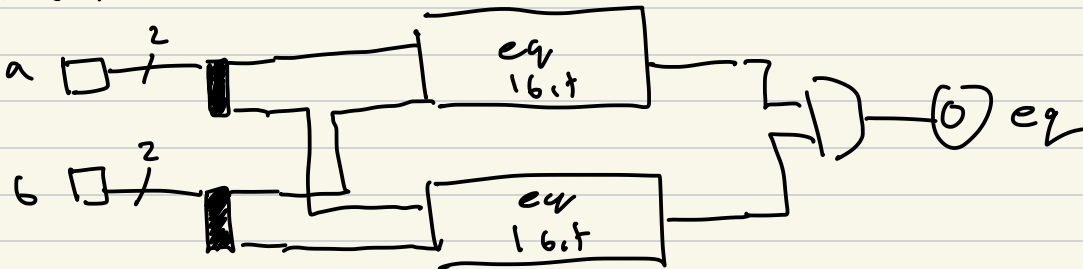
XNOR

1
0
0
1

1 bit comparator

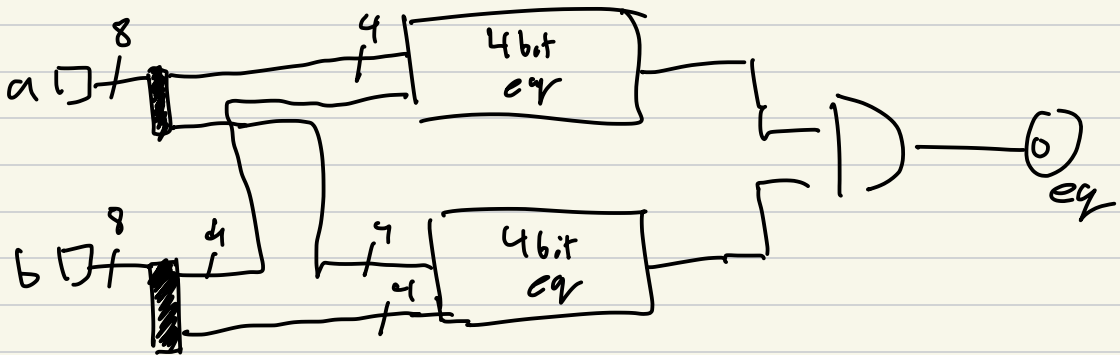


2-bit comparator

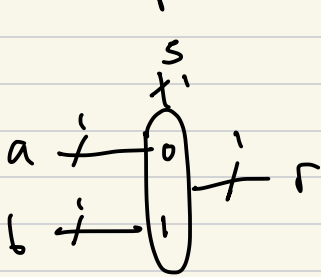


N-bit Comparators

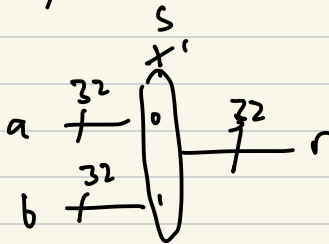
8 bit comparator



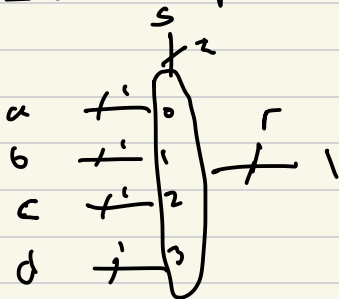
Multiplexor (MUX)



1 bit 2 input MUX



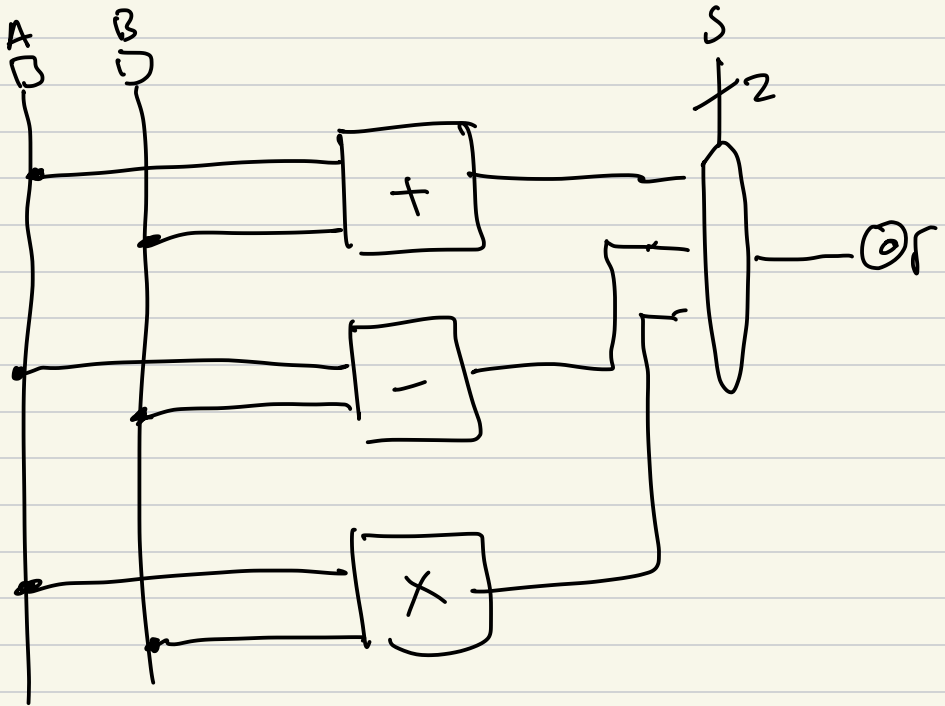
32 bit 2 input MUX



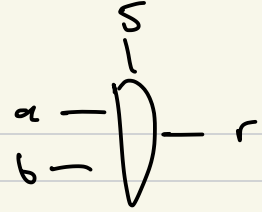
1 bit 4 input MUX

Uses of MUXes

ALU Arithmetic Logic Unit



Implementing MUXes



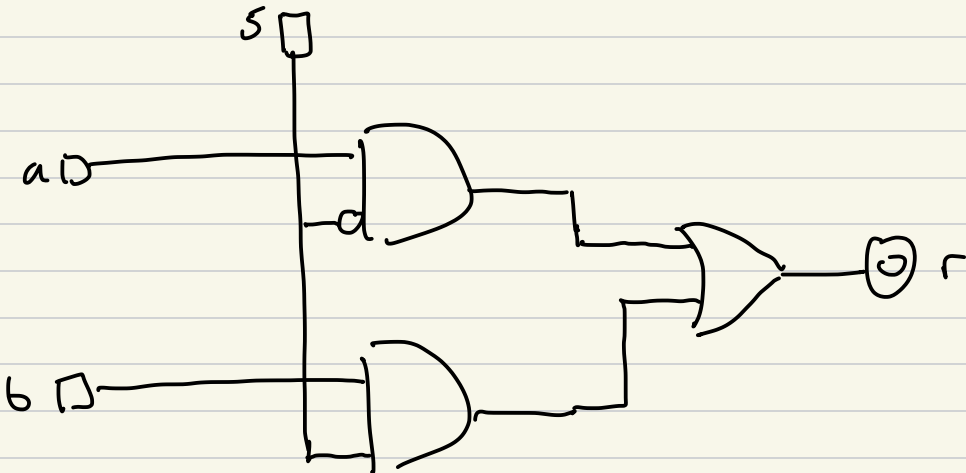
1 bit 2 input MUX

a	b	s	r
0	0	0	0
0	0	1	0
0	1	0	0
✓ 0	1	1	1
✓ 1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

$$r = (\bar{a} \cdot b \cdot s) + (a \cdot \bar{b} \cdot \bar{s}) + (a \cdot b \cdot \bar{s}) + (a \cdot b \cdot s)$$

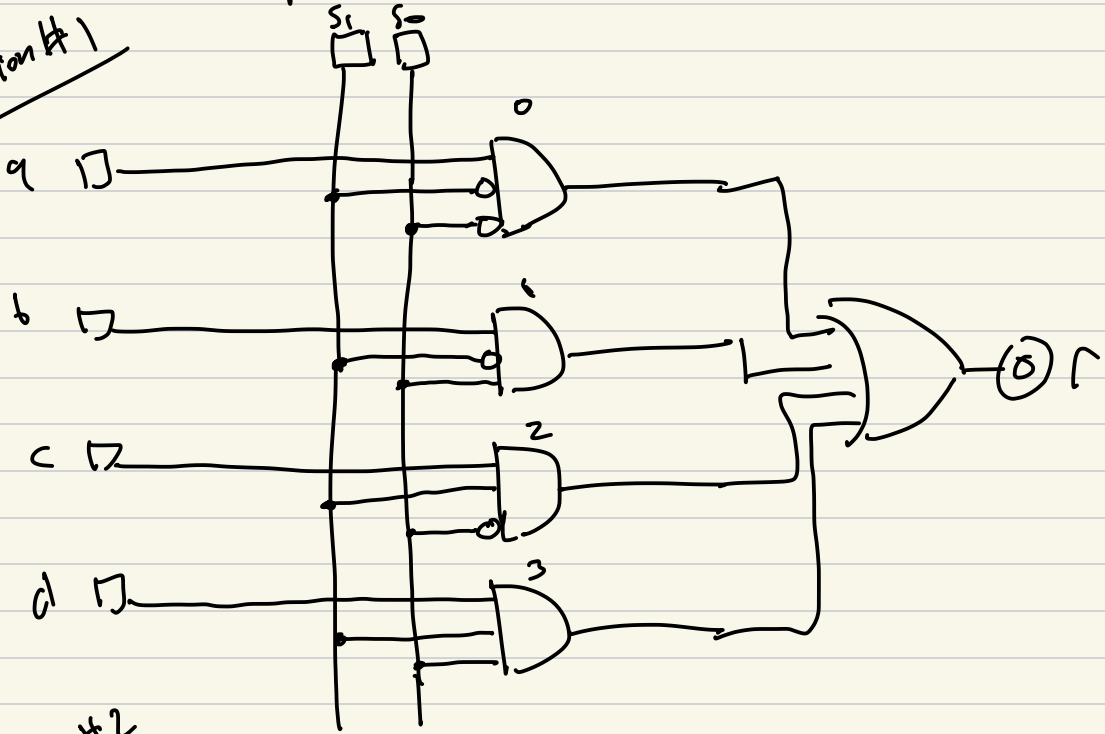
} circuit

Direct implementation

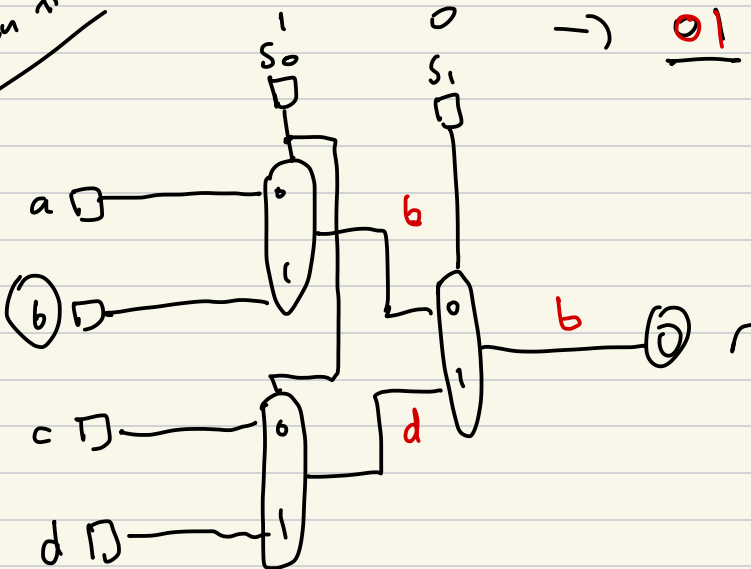


1 b.1 4 input MUX

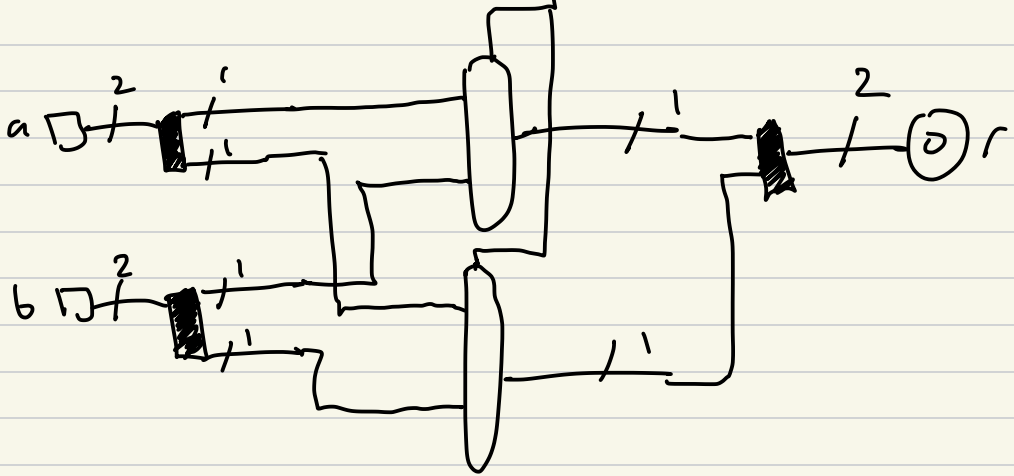
option #1



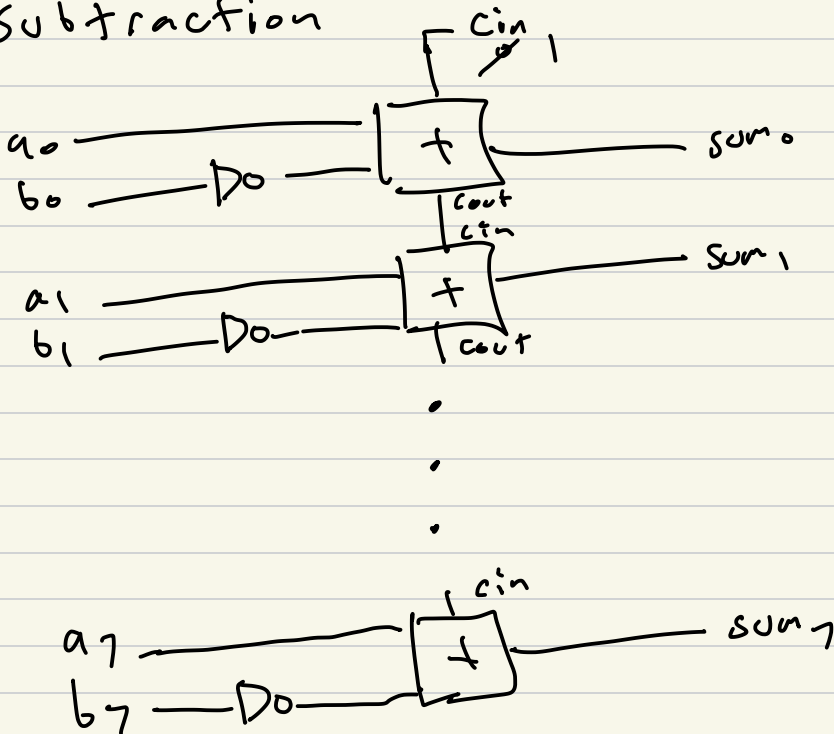
option #2



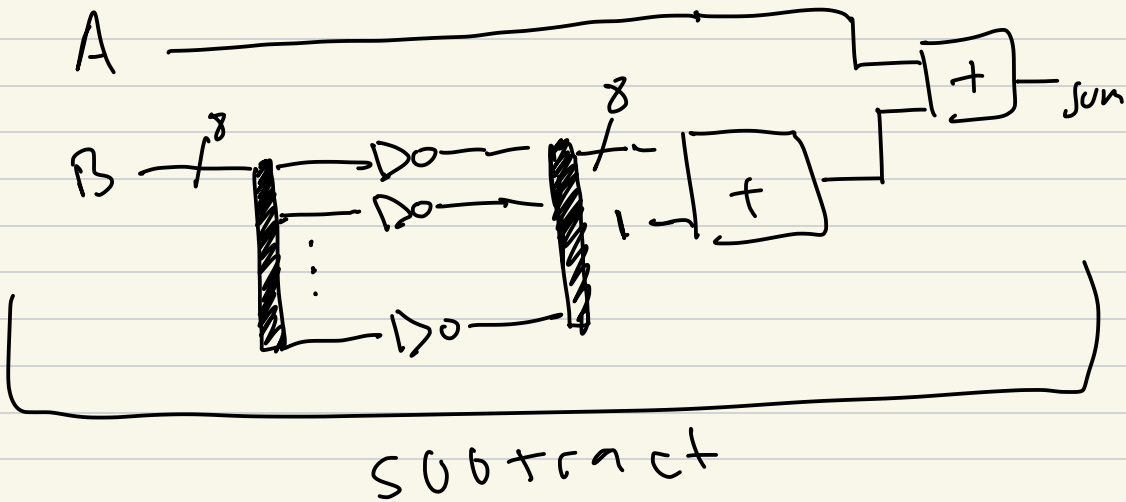
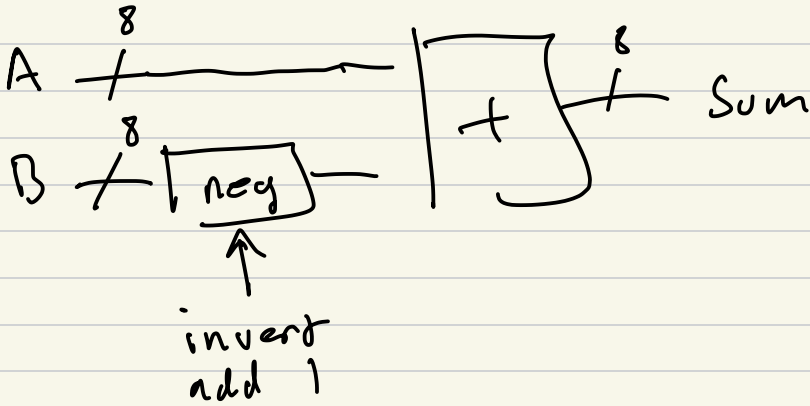
2 bit 2 input MUX SD

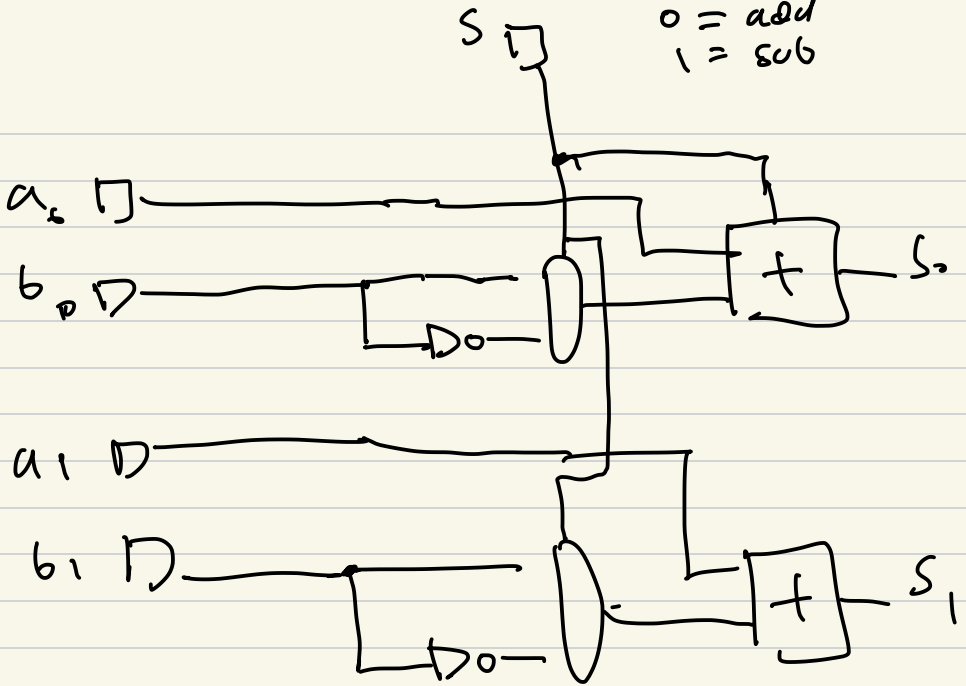


Subtraction



$$A - B = A + (-B)$$





Sequential Logic

